Power MOSFET Single-Shot and Repetitive Avalanche Ruggedness Rating

Introduction

Electronic applications have progressed significantly in recent years and have inevitably increased the demand for an intrinsically rugged power MOSFET. Device ruggedness is defined by the capacity of a device to sustain an avalanche current during an unclamped inductive load switching event. However, the avalanche ruggedness performance of a power MOSFET is normally measured within the industry as a single-shot unclamped inductive switching (UIS) avalanche energy or E_{AS}. Whilst this provides an easy and quick method of quantifying the robustness of a MOSFET in avalanche, it does not necessarily reflect the true device avalanche capability[1-3] in an application.

This note explains the fundamentals of UIS operation and reviews the appropriate method of quantifying the safe operating condition for a power MOSFET subjected to UIS operating condition. The note also covers the much-discussed repetitive avalanche ruggedness capability and how this operation can be quantified to operate safely.

Understanding Power MOSFET Single-shot Avalanche Event

Single shot avalanche capability of a device has been well established by both researchers and the industry[1-3]. The test can be carried out on a simple unclamped inductive load switching circuit as shown in Figure 1.

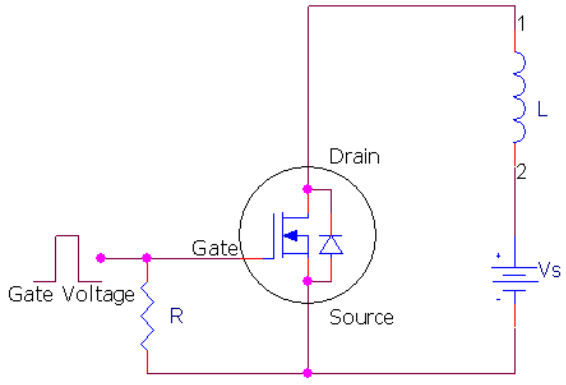

Figure 1. Unclamped inductive load test circuit for MOSFET ruggedness evaluation.

Single-Shot UIS Operation:-

A voltage pulse is applied to the gate to turn the MOSFET ON as shown in Figure 2a. This allows the load current to ramp up according to the inductor value, L and the drain supply voltage, V_S as shown in Figures 2b and 2c. At the end of the gate pulse, the MOSFET is turned OFF. The current in the inductor continues to flow causing the voltage across the MOSFET to rise sharply. This over-voltage is clamped at breakdown voltage, V_{BR} until the load current reaches zero as illustrated in Figure 2b. Typically V_{BR} is:

$$V_{BR} \approx 1.3 \times BV_{DSS} \quad \textbf{[1]}$$

The peak load current passing through the MOSFET before turn OFF will be the single-shot avalanche current, I_{AS} of the UIS event as illustrated in Figure 2c. The rate at which the avalanche current decays is dependent on inductor value and can be determined by:

$$\frac{dI_{AS}}{dt_{AV}} = -\frac{V_{BR} - V_S}{L} \quad \textbf{[2]}$$

The peak avalanche power, $P_{AV(pk)}$ dissipated in the MOSFET shown in Figure 2d is a product of the breakdown voltage, V_{BR} and the avalanche current, I_{AS} as shown in Figures 2b and 2c respectively. The avalanche energy dissipated is the area under the P_{AV} waveform and can be estimated from the following expression:

$$E_{AS} = \frac{P_{AV(pk)} \times t_{AV}}{2} \quad \textbf{[3.1]}$$

or

$$E_{AS} = \frac{1}{2} \cdot \frac{V_{BR}}{V_{BR} - V_S} \cdot LI_{AS}^2 \quad \textbf{[3.2]}$$

Another crucial parameter involved in a MOSFET avalanche event is the junction temperature. The transient junction temperature rise during device avalanching at a time after the beginning of the avalanche event, τ can be determined by the following expression:

$$T_{jrise}(\tau) = \int_0^{\tau} P_{AV}(t) \frac{dZ_{th(\tau - t)}}{dt} dt \quad \textbf{[4]}$$

where Z_{th} is the power MOSFET transient thermal impedance. Alternatively, the maximum T_{jrise} can be approximated by:

$$T_{jrise(\max)} \approx \frac{2}{3} P_{AV(pk)} Z_{th(t_{AV}/2)} \quad \textbf{[5]}$$

(*Assuming $T_{j(max)}$ occurs at t_{AV}/2*)

where $Z_{th(t_{AV}/2)}$ is the device transient thermal impedance at half the t_{AV} period

The maximum junction temperature resulting from the avalanche event will therefore be:

$$T_{j(\max)} \approx T_{jrise(\max)} + T_j \quad \textbf{[6]}$$

where T_j refers to the junction temperature prior to turn OFF.

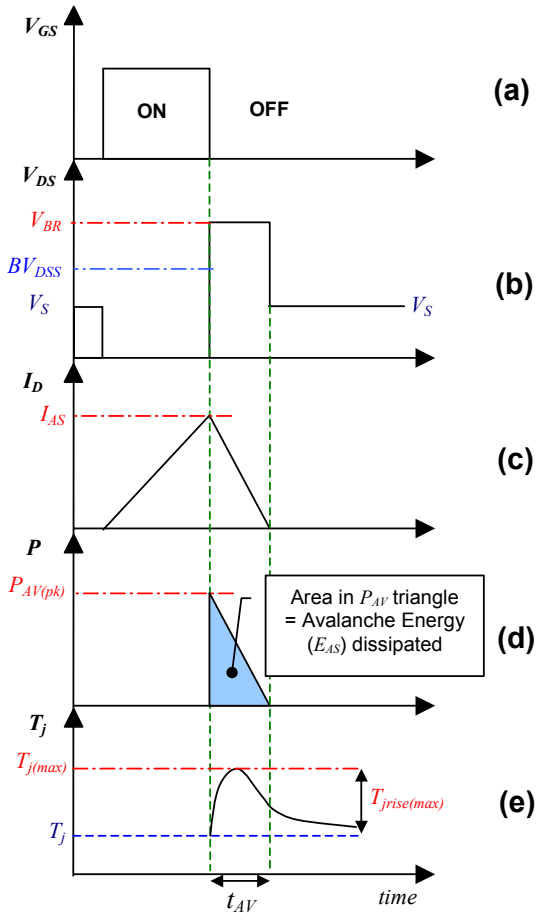

Figure 2. Single-shot UIS waveforms (**a**) Gate pulse, V_{GS} (**b**) MOSFET Drain-Source Voltage, V_{DS}, (**c**) Current passing through MOSFET, I_D, (**d**) Peak avalanche power, $P_{AV(pk)}$ and (**e**) Transient junction temperature profile of MOSFET during an avalanche event.

Single-Shot Avalanche Ruggedness Rating

The failure mechanism for a single-shot avalanche event in a power MOSFET is known to be due to the junction exceeding a maximum temperature above which catastrophic damage is done to the MOSFET. If the transient temperature resulting from an avalanche event, as illustrated in Figure 2e, rises beyond a recommended rated value, the device risks being degraded. The recommended rated value is derated from the maximum temperature for optimum reliability.

Blackburn[2] has discussed a general guideline in detail on the appropriate method of quantifying the single-shot avalanche capability of a device by taking avalanche current and initial junction temperature into consideration. Safe operation for a device single-shot UIS event can be defined by a maximum allowed avalanche current as a function of avalanche time. The maximum allowed avalanche current is set so that a safe maximum junction temperature, $T_{j(max)}$ of 175°C is never exceeded. Using equation [6], Figure 3 can be plotted.

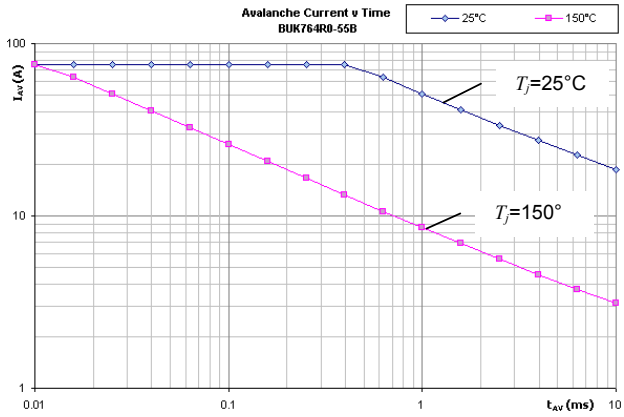

Figure 3. Single-shot avalanche ruggedness SOAR curves of BUK764R0-55B limited to a $T_{j(max)}$ of 175°C.

Figure 3 shows the SOAR curves of a device single-shot avalanche capability. The 25°C junction temperature curve shows the maximum allowable I_{AS} for a given t_{AV} at an initial T_j of 25°C. This maximum I_{AV} will give rise to a maximum junction temperature, $T_{jrise(max)}$ of 150°C resulting in a $T_{j(max)}$ of 175°C. The area under the SOAR curve will be the safe operating area (SOA). Similarly the 150°C junction temperature curve will be the maximum operating limit for an initial T_j of 150°C. The $I_{AS(max)}$ will induce a $T_{jrise(max)}$ of 25°C resulting in a $T_{j(max)}$ of 175°C. Again the area under the curve will be the SOA.

The maximum junction temperature resulting in catastrophic device avalanche failure is approximately 380°C, which is well in excess of the rated $T_{j(max)}$ of 175°C. However, operating beyond the rated $T_{j(max)}$ may induce long-term detrimental effects to the power MOSFET and is not recommended.

Understanding Power MOSFET Repetitive Avalanche Event

Repetitive avalanching simply refers to an operation involving repeated single-shot avalanche events as discussed earlier. Until recently, most manufacturers have avoided the issues pertaining to the power MOSFET repetitive avalanche capability. This is primarily due to the complexity in such operation and the difficulties in identifying the underlying physical degradation process in the device.

Due to the traumatic nature of the avalanche event, a repetitive avalanche operation can be hazardous for a MOSFET, even when individual avalanche events are well below the single shot UIS rating. This type of operation involves additional parameters such as the frequency, duty-cycle and the thermal resistance, R_{th} of the application during the repetitive avalanche event. However, it is possible to derate the single shot rating to define a repetitive avalanche safe operating area.

Repetitive UIS Operation:-

Referring to Figure 1., in a repetitive UIS test the gate is fed with a train of voltage pulses at frequency, f for a duty cycle as shown in Figure 4a. The resulting breakdown voltage, V_{BR} and current passing through the load, I_D are the same as for a single-shot UIS except that the peak I_D will now be denoted as repetitive avalanche current, I_{AR} as shown in Figure 4b.

To obtain the average repetitive avalanche power dissipated, $P_{AV(R)}$ resulting from the repetitive UIS operation as shown in Figure 4c. It is necessary to first calculate the E_{AS} for a single avalanche event using equation [3]. Subsequently substituting E_{AS} into the expression gives:

$$P_{AV(R)} = E_{AS} \times f \qquad [7]$$

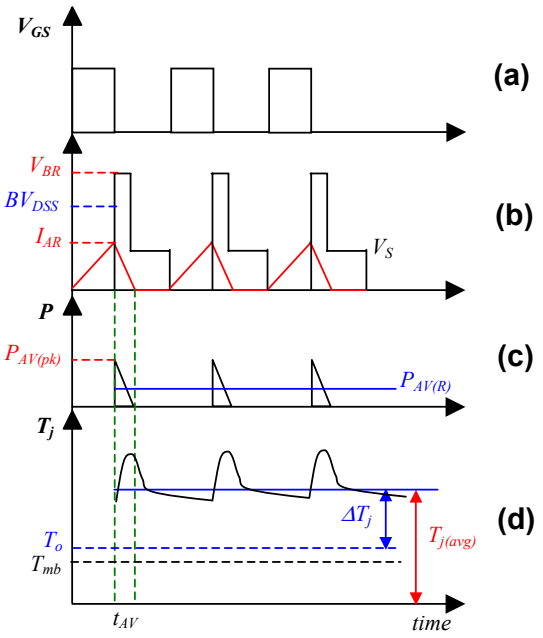

Figure 4. Repetitive UIS waveforms (**a**) Gate pulse, V_{GS} (**b**) MOSFET Drain-Source Voltage, V_{DS} and repetitive avalanche current, I_{AR}, (**c**) Repetitive avalanche power $P_{AV(R)}$ and (**d**) Transient junction temperature components of MOSFET during repetitive avalanching.

Temperature Components

The temperature rise from the repetitive avalanching mode in the power MOSFET can be defined as shown in Figure 4d.

The temperature, T_o comprises the mounting base temperature, T_{mb} and the temperature rise resulting from any ON state conduction, T_{cond}.

$$T_O = T_{mb} + T_{cond} \qquad [8]$$

In addition there is a steady-state average junction temperature rise, ΔT_j resulting from the average repetitive avalanche power loss.

$$\Delta T_j = P_{AV(R)} \times R_{th(j-amb)} \qquad [9]$$

where $R_{th(j-amb)}$ is the thermal resistance of the device in the application. The summation of equations [8] and [9] will give the average junction temperature, $T_{j(avg)}$ of a power MOSFET in repetitive UIS operation.

$$T_{j(avg)} = T_O + \Delta T_j \qquad [10]$$

Repetitive Avalanche Ruggedness Rating

Following extensive investigation, it is clear that there is more than one failure or wear-out mechanism involved in repetitive avalanching. Temperature is **NOT** the only limiting factor to a repetitive avalanche operation. However, by limiting the temperature together with the repetitive avalanche current, I_{AR}, it is possible to define an operating environment such that the avalanche conditions do not activate any device degradation. This allows the power MOSFET to operate under repetitive UIS conditions safely.

Figure 5 shows the avalanche SOAR curves for BUK764R0-55B where 'Rep. Ava' represents the repetitive avalanche SOAR curve.

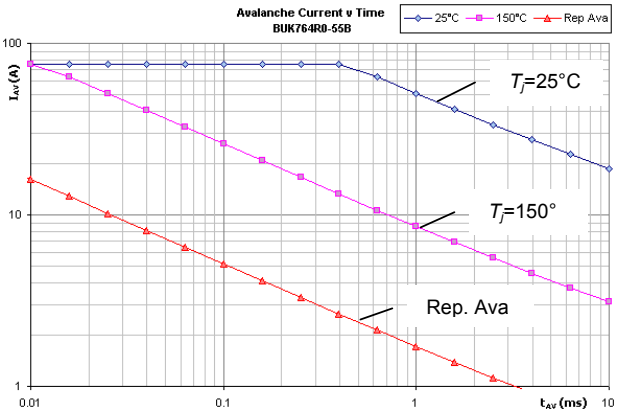

Figure 5. Single-shot (Initial T_j = 25°C and 150°C) and repetitive (Rep. Ava) avalanche ruggedness SOAR curves of BUK764R0-55B limited to a $T_{j(max)}$ of 175°C and a $T_{j(avg)}$ of 170°C respectively.

The two conditions which must be satisfied for safe operation of a power MOSFET under repetitive avalanching mode are as follows:-

1. I_{AR} should **NOT** exceed the Repetitive Avalanche SOAR Curve.
2. The $T_{j(avg)}$ should **NOT** exceed 170°C.

Conclusion

Power MOSFETs can sustain single-shot and repetitive avalanche events. Simple design rules and SOAR regions have been provided.

EXAMPLES

The following examples examine cases of avalanche operation acceptance evaluation.

Single-shot Avalanche Case

Device = BUK764R0-55B [refer to Figure 5]
L = 2mH
I_{AS} = 40A
$R_{th(j-amb)}$ = 5K/W

Step 1
From the above information, t_{AV} can be determined using equation [2], which in this case is 1.11ms. Transferring the I_{AV} and t_{AV} conditions onto Figure 5. The operating point is under the T_j = 25°C SOAR curve but over the T_j = 150°C SOAR curve suggesting the operating condition maybe feasible.

Step 2
To check, calculate the $T_{jrise(max)}$ using equation [5], where $Z_{th(556\mu s)}$ on the datasheet is approximately 0.065K/W. This will give a $T_{jrise(max)}$ of 124.8°C.

Based upon the above calculations the operating condition is acceptable if the device T_j < 50°C.

Repetitive Avalanche Case

Device = BUK764R0-55B [refer to Figure 5]
L = 0.5mH
I_{AR} = 6A
f = 3kHz
$R_{th(j-amb)}$ = 5K/W
T_O = 100°C

Step 1
From the above information, t_{AV} can be determined using equation [2], which in this case is ~0.042ms. Transferring the I_{AV} and t_{AV} conditions onto Figure 5. The operating point is under the boundary of the Rep. Avalanche SOAR curve suggesting the operating condition is acceptable.

Condition 1 achieved.

Step 2
Calculate the Single-shot avalanche energy dissipation, E_{AS} using equation [3]. (E_{AS} = 9mJ)

Step 3
Calculate the average repetitive avalanche power, $P_{AV(R)}$ using equation [7]. ($P_{AV(R)}$ = 27W)

Step 4
Calculate the average ΔT_j rise from repetitive avalanche, ΔT_j using equation [9]. (ΔT_j = 135°C)

Step 5
Determine the average junction maximum temperature in repetitive avalanche operation, $T_{j(avg)}$ using equation [10]. ($T_{j(avg)}$ = 235°C)

Condition 2 not achieved.

Based on the above calculations, the operating conditions satisfied the first but not the second requirement for safe repetitive avalanche operation. This was because the maximum $T_{j(avg)}$ exceeded 170°C.

Solution
To make the above operation viable, the design engineer has to achieve the 2nd condition by reducing the $T_{j(avg)}$.

This can be achieved simply by improving the heat sinking of the device. Reducing the $R_{th(j-amb)}$ from 5K/W to 2.5K/W will give a $T_{j(avg)}$ of 167.5°C satisfying condition 2 of safe repetitive avalanche operation.

References:

1. **D.L. Blackburn**, *"Turn-off Failure of Power MOSFETs"*, Proc. 1985 IEEE Power Electronics Specialists Conference, pp 429-435, June 1985.
2. **D.L. Blackburn**, *"Power MOSFET Failure Revisited"*, Proc. 1988 IEEE Power Electronics Specialists Conference, pp 681-688, April 1988.
3. **Rodney R. Stoltenburg**, *"Boundary of Power-MOSFET, Unclamped Inductive-Switching (UIS) Avalanche-Current Capability"*, Proc. 1989 Applied Power Electronics Conference, pp 359-364, March 1989.

Symbols:

BV_{DSS}	Device rated breakdown voltage
E_{AS}	Single-shot avalanche energy
I_D	MOSFET Drain current
I_{AS}	Single-shot avalanche current
I_{AR}	Repetitive avalanche current
I_{AV}	Avalanche current
L	Inductor
$P_{AV(pk)}$	Peak avalanche power
$P_{AV(R)}$	Average repetitive avalanche power
R_{th}	Device thermal resistance
$R_{th(j\text{-}amb)}$	Device junction to ambient thermal resistance
T_o	Initial temperature, summation of T_{mb} & T_{cond}
T_{cond}	ON-state conduction temperature
T_j	Junction temperature
T_{jrise}	Junction temperature rise
$T_{jrise(max)}$	Maximum junction temperature rise
$T_{j(max)}$	Maximum Junction temperature
$T_{j(avg)}$	Average junction temperature (For repetitive avalanche)
T_{mb}	Mounting base/case temperature
ΔT_j	Average temperature rise from average repetitive avalanche power loss
t_{AV}	Avalanche period/duration
V_{BR}	Breakdown voltage
V_{DS}	MOSFET Drain-Source voltage
V_{GS}	MOSFET Gate-Source voltage
V_S	Supply voltage
Z_{th}	Device Transient thermal impedance
$Z_{th(t_{AV}/2)}$	Device Transient thermal impedance measured at half the avalanche period.